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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

STEVENS, THOMAS H

ART UNIT	PAPER NUMBER
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2123

DATE MAILED: 10/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/017,506

Applicant(s)

KOPPL ET AL.

Examiner

Thomas H. Stevens

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 August 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. Claims 1-9 were examined.

Section I: Final Rejection

Claim Rejections - 35 USC § 102

2. Claims 1-5,8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Wilkinson et al ("Assessment of UHF Power Amplifier Linearization by Measurement and Simulation (IEEE 1989)). Wilkinson et al., teaches a communication system simulator for nonlinear signals coupled with Volterra series representation (abstract).

Claim 1. A simulation method (title) determining nonlinear signal distortion (pg. 60, right column, lines 1-5) in an analog circuit , which is to be tested, for processing discrete multitone signals (DMT), with the simulation method having the following steps: applying a discrete multitone signal, (abstract) which has a number of uniformly spaced carrier for data transmission in range, the analog be tested (pg. 60, right column, 6th paragraph), and to digital filter suppression the output signal from the analog circuit , (pg.62, right column, 1st paragraph) which be tested, from the output signal from the digital filter order to produce a difference signal, (c) adjustment of the filter until the difference signal a minimum, with the adjusted digital filter forming an equivalent circuit of the analog circuit (a plurality of FETs: pg.62, right column, 1st paragraph; pg. 60, left column 5th paragraph, lines 3-5)) (d) application the discrete multitone signal to the adjusted digital filter with least carrier frequency being suppressed, for measuring the intermodulation product of the adjusted digital filter (pg. 62, left column, paragraph 7)

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Claim 2. The simulation method as claimed in claim 1 (title; pg.62, right column, 1st paragraph) wherein multitone signal calculated from the measured intermodulation product (title; pg.62, right column, 1st paragraph).

Claim 3. The simulation method in claim 1 or 2, (title; pg.62, right column, 1st paragraph) wherein the adjustable modeling filter discrete-time Volterra filter (abstract), or a neural network.

Claim 4. The simulation method as claimed of the preceding claims, (title; pg.62, right column, 1st paragraph) wherein the adjustable modeling filter (Design choice: making adjustable; see *In re Stevens*, 212 F.2d 197, 101 USPQ 284 (CCPA 1954)) is connected in parallel with the analog circuit, which is to be tested.

Claim 5. The simulation method as claimed in one the preceding claims, (title; pg.62, right column, 1st paragraph) wherein adjusted modeling filter (Design choice: making adjustable; see *In re Stevens*, 212 F.2d 197, 101 USPQ 284 (CCPA 1954)), which forms equivalent circuit of analog circuit connected to further adjusted modeling filters, which form equivalent circuits further analog circuits, in order generate an overall equivalent circuit for an analog overall circuit (pg. 60, left column, 5th paragraph).

Claim 8. A test arrangement for determining nonlinear (abstract) signal distortion (pg. 60, right column, lines 1-5) of analog circuit elements of signal processing circuit for

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signal processing of DMT signals having: (a) a signal generator for producing a discrete multitone signal (b) (abstract) adjustable modeling filters (Design choice: making adjustable; see *In re Stevens*, 212 F.2d 197, 101 USPQ 284 (CCPA 1954)) which are each connected in with associated analog circuit element (a plurality of FETs: pg.62, right column, 1st paragraph; pg. 60, left column 5th paragraph, lines 3-5)) , with the signal inputs of the modeling filters and of the analog circuit elements being connected to the signal generator (c) subtraction circuits, which each subtract the output from a modeling filter from the output signal from the associated analog circuit element in order to form a difference signal; (d) an adjustment circuit, which compares the difference signals with a nominal value and adjust the modeling filters (Design choice: making adjustable; see *In re Stevens*, 212 F.2d 197, 101 USPQ 284 (CCPA 1954)) until the difference signals match the nominal value (pg. 61, left column, last paragraph, lines 16-19); and having (e) a measurement circuit, which is connected to the outputs of the modeling filters (pg. 61, right column, lines 19-28) for measuring the interconnection products (pg. 62, left column, paragraph 7) of the adjusted modeling filters .

Claim 9. The test arrangement as claimed in claim 8, (abstract) wherein the test circuit is followed by a calculation circuit (32) for calculating the multitone signal power ratio of the output signals, which are emitted from the modeling filter (examiner assumes applicants are disclosing pg.6, lines 24-30 of the specification: pg. 62, left column, 4th paragraph).

Claim Rejections - 35 USC § 103

3. Claim 6 and 7 are rejected under 35 U.S.C. 103 (a) as obvious by Wilkinson et al., (IEEE 1989), in view of Hjartarson et al., (U.S. Patent 6,295,343 (2001)). Wilkinson et al., teaches a communication system simulator for nonlinear signals coupled with Volterra series representation (abstract) that encompass negating AM distortion in AM circuits; but doesn't teach specific AM circuits.

Hjartarson et al. teaches a method and apparatus for combining voice card and XDSL line card functions with subscriber line interface circuit (SLIC) and digital subscriber lines (DSL).

At the time of invention, it would have been obvious to one of ordinary skill in the art to modify Wilkinson et al., with Hjartarson et al. since separation of signals in a network (Hjartarson: column 2, lines 26-30), particular AM clear voice (Hjartarson: column 1, lines 20-25) is imperative for AM system performance (Wilkinson: pg. 60, left column, 1st paragraph and right column 1st column).

Claim 6. The simulation method as claimed preceding claims, (Wilkinson: title; pg.62, right column, 1st paragraph) wherein the analog overall circuit a DSL-SLIC circuit (Hjartarson: column 5, lines 5-15).

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Claim 7. The simulation method as claimed one of the preceding claims, (Wilkinson: title; pg.62, right column, 1st paragraph ; Hjartarson: column 5, lines 5-15) wherein discrete multitone signals are generated in a signal generator (1).

Section II: Response to Applicants' Arguments (1st Office Action)

Specification/ Improper Multiple Dependent Claims

4. Applicants are thanked for addressing this issue. Objections are withdrawn.

102(b)

5. Applicants are thanked for addressing this issue. Applicants state the prior art is silent regarding generation of a difference signal by subtracting the output signal, etc. (applicants' response pg.7, 4th paragraph lines 1-4). Examiner refutes this statement by declaring the existence of difference frequencies as inherent to the process of eliminating intermodulation products (i.e., $2f_1 \pm 2f_2$), which is ubiquitous within the art. Furthermore, examiner cites law case of *In re Garza*, 274 F.2d 669, 124, USPQ 378 (CCPA 1960) that details duplication of parts in response applicants' argument regarding a "second discrete multitone signal", coupled with *In re Stevens*, 212 F.2d 197, 101 USPQ 284 (CCPA 1954)) regarding the limitation of "adjustable".

Applicants state the prior art fails to teach nonlinear signal distortion for analog circuits (applicants' arguments, pg. 8, 2nd paragraph). The prior art discloses the AM/AM distortion (pg. 60, right column, paragraph s 1-6) using non-linear models (pg. 60, left column, 3rd paragraph) with circuits (Field Effect Transistors (FETS) (pg. 62,

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right column 1st paragraph; FET are common in electronic circuits for analog or digital communications).

Applicant were silent in response to rejections to claim 9.

Summarily, the rejection stands.

103(a)

6. Applicants were silent in rebuttal to claims 6 and 7, thus rejection stands.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

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Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm) or contact Supervisor Mr. Leo Picard at (571) 272-3749. Central Fax number is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.


Paul L. Rodriguez 10/6/05
Primary Examiner
Art Unit 2125

October 4, 2005

THS